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1 **Self-checking alternating logic: Sequential circuit design**
Scott E. Woodard, Gernot Metze
April 1978 **Proceedings of the 5th annual symposium on Computer architecture ISCA '78**
Publisher: ACM Press
Full text available: pdf(711.57 KB) Additional Information: full citation, abstract, references, index terms

There has been considerable study of the tradeoff between improved reliability and additional hardware. An alternative is to trade speed for improved reliability, as in alternating logic, which is based on the successive execution of a function and its dual. In addition to doubling time, this approach involves an increase in hardware which, however, is generally modest compared to the usual hardware redundancy approaches. This paper will explore recent advances in the design of sequential c ...

2 **Design methodology and microdiagnostics development for a self-checking microprocessor**
R. A. Parekhji, N. K. Nanda
August 1989 **ACM SIGMICRO Newsletter , Proceedings of the 22nd annual workshop on Microprogramming and microarchitecture MICRO 22**, Volume 20 Issue 3
Publisher: ACM Press
Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, index terms

The conventional design of electronic circuits is intolerant to operational faults. Self-checking logic is aimed at online fault detection and can hence be incorporated to achieve reliable operation. In this paper, the design of a self-checking microprocessor is discussed. Self-checking strategies for different functional units are selectively and judiciously applied, and also modified wherever necessary, for the design of the register section, the arithmetic & logic unit and the contro ...

3 **Security and correctness: Self-checking instructions: reducing instruction redundancy for concurrent error detection**
Sumeet Kumar, Aneesh Aggarwal
September 2006 **Proceedings of the 15th international conference on Parallel architectures and compilation techniques PACT '06**
Publisher: ACM Press
Full text available: pdf(266.40 KB) Additional Information: full citation, abstract, references, index terms

With reducing feature size, increasing chip capacity, and increasing clock speed, microprocessors are becoming increasingly susceptible to transient (soft) errors.

Redundant multi-threading *(RMT)* is an attractive approach for concurrent error detection. However, redundant thread execution has a significant impact on performance and energy consumption in the chip.In this paper, we propose reducing instruction redundancy (the instructions that are redundantly executed) as a means to mitigat ...

Keywords: RISC/CISC, VLIW architectures, concurrent error detection, reducing instruction redundancy, redundant multi-threading, self-checking instructions

4 On the design of self-checking functional units based on Shannon circuits

Michele Favalli, Cecilia Metra

January 1999 **Proceedings of the conference on Design, automation and test in Europe DATE '99**

Publisher: ACM Press

Full text available: pdf(84.35 KB) Additional Information: full citation, index terms

5 Design of self-checking software

S. S. Yau, R. C. Cheung

April 1975 **ACM SIGPLAN Notices , Proceedings of the international conference on Reliable software**, Volume 10 Issue 6

Publisher: ACM Press

Full text available: pdf(688.95 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses different techniques for constructing a piece of self-checking software for systems where ultra-reliability is required. Self-checking software can be designed to detect software errors, to locate and to stop the propagation of software errors, to assist in the recovery from errors and to verify the integrity of the system. Self-checking techniques can be implemented in the program to check the function, the control sequence and the data of a process. The functional asp ...

6 A CAD framework for generating self-checking multipliers based on residue codes

I. Alzaher Noufal, M. Nicolaidis

January 1999 **Proceedings of the conference on Design, automation and test in Europe DATE '99**

Publisher: ACM Press

Full text available: pdf(91.96 KB) Additional Information: full citation, index terms

Keywords: fault secure circuits, multipliers, residue arithmetic codes, self-checking circuits

7 Area versus detection latency trade-offs in self-checking memory design

O. Kebichi, Y. Zorian, M. Nicolaidis

March 1995 **Proceedings of the 1995 European conference on Design and Test EDTC '95**

Publisher: IEEE Computer Society

Full text available: pdf(608.50 KB) Publisher Site Additional Information: full citation, abstract, citings

With the increasing need for on-line reliability today's electronic systems often require certain levels of self-checking. Depending on its application, the level of self-checking, i.e. the detection latency, of a given system is determined. Most of the known on-line testing

schemes provide a fixed level of self-checking, hence do not allow flexibility in meeting the allowed detection latency and hardware overhead. This paper presents a new self-checking scheme for memories (RAMs, ROMs, etc.), w ...

Keywords: BIST, RAMs, ROMs, built-in self test, concurrent testing, design for testability, detection latency, hardware cost, hardware overhead, integrated circuit testing, integrated memory circuits, random-access storage, read-only storage, self-checking memory design, system requirements

8 Testing and Fault-Tolerance: Self-checking sequential circuits with self-healing ability

Ilya Levin, Vladimir Ostrovsky, Sergey Ostanin, Mark Karpovsky

April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI GLSVLSI '02**

Publisher: ACM Press

Full text available: pdf(218.55 KB) Additional Information: full citation, abstract, references, index terms

In this paper we deal with totally self-checking (TSC) synchronous sequential circuits (SSCs), that are able to recover after an occurrence of a fault. We call SSC owing this property as a self-healing SSC. A concept of a partially monotonic SSC is used in the paper. It is shown that the partially monotonic SSCs satisfy the self-healing property. A novel *reduced m-out-of-n* code is developed. It is proposed applying this code to the synthesis of a TSC checker for the state monotonic SSCs. ...

9 Logic simulation and fault analysis of a self-checking switching processor

H. Y. Chang, R. C. Dorr, R. A. Elliott

June 1972 **Proceedings of the 9th workshop on Design automation DAC '72**

Publisher: ACM Press

Full text available: pdf(542.26 KB) Additional Information: full citation, abstract, references, index terms

During an exploratory study in the design of a stored program processor for an electronic switching system, the need for logic simulation for design verification was evident [1]. The advantages of using logic simulation concurrent with hardware design are many. This paper will discuss logic simulation and fault analysis work undertaken while designing a self-checking switching processor. The logic simulation and fault analysis were implemented on an IBM/360 model 67 executing a s ...

10 Design automation of self checking circuits

S. M. Kia, Sri Parameswaran

September 1994 **Proceedings of the conference on European design automation EURO-DAC '94**

Publisher: IEEE Computer Society Press

Full text available: pdf(563.97 KB) Additional Information: full citation, references, citings, index terms

11 Self-Checking Scheme for the On-Line Testing of Power Supply Noise

C. Metra, L. Schiano, B. Riccò, M. Favalli

March 2002 **Proceedings of the conference on Design, automation and test in Europe DATE '02**

Publisher: IEEE Computer Society

Full text available: pdf(107.82 KB) Additional Information: full citation, abstract

We propose a self-checking scheme for the on-line testingof power supply noise exceeding a tolerance bound tobe chosen accordingly to system's constraints. Upon the occurrenceof such a noise, our scheme provides an output errormessage, which can be exploited for diagnosis purposesor to recover from the detected noise (thus guaranteeing thesystem's correct operation). As far as we are concerned, noon-line testing scheme for

power supply noise has been proposedup to now. Our scheme negligibly impa ...

12 Problems Due to Open Faults in the Interconnections of Self-Checking Data-Paths
M. Favalli, C. Metra
March 2002 **Proceedings of the conference on Design, automation and test in Europe DATE '02**
Publisher: IEEE Computer Society
Full text available: pdf(104.56 KB) Additional Information: full citation, abstract

In this work, the problem of open faults affecting the inter-connectionsof SC circuits composed by data-path and controlis analyzed. In particular, it is shown that, in case opensaffect control signals, some problems may arise even if bothcontrol and data-path signals are concurrently checked. Inparticular, wrong codewords may be generated at the outputsof multiplexers and registers. To address this problem, newregisters and multiplexers are proposed which allow the designdata-paths which are TS ...

13 A high-level synthesis approach to optimum design of self-checking circuits
M. Sami, A. Antola, V. Piuri
September 1996 **Proceedings of the conference on European design automation EURO-DAC '96/EURO-VHDL '96**
Publisher: IEEE Computer Society Press
Full text available: pdf(99.63 KB) Additional Information: full citation, references, citings, index terms

14 A Totally Self-checking 1-out-of-3 Code Error Indicator
Antonis Paschalis, Nikos Gaitanis, Dimitris Gizopoulos, Panagiotis Kostarakis
March 1997 **Proceedings of the 1997 European conference on Design and Test EDTC '97**
Publisher: IEEE Computer Society
Full text available: pdf(604.42 KB) Publisher Site Additional Information: full citation, abstract

In this paper, an asynchronous TSC 1-out-of-3 (1/3) code error indicator is introduced that memorises erroneous 1/3 code inputs {000, 011, 101, 110, 111} with time duration greater than a discrimination time T. Such an error indicator is used to discriminate transient erroneous 1/3 code inputs from real ones as well as to detect not only faults that cause logical errors but also delay faults (short or long) that alter the circuit delay outside its specified limits (upper or lower bounds) without ...

Keywords: totally self checking (TSC), circuits, 1-out-of-3 code, error indicator

15 Self-checking architectures for fast Hartley transform
J. M. Tahir, S. S. Dlay, R. N. G. Naguib, O. R. Hinton
March 1995 **Proceedings of the 1995 European conference on Design and Test EDTC '95**
Publisher: IEEE Computer Society
Full text available: pdf(680.50 KB) Publisher Site Additional Information: full citation, abstract

For many real-time and scientific applications, it is desirable to perform signal and image processing algorithms by means of special hardware in very high speed. With the advent of VLSI technology, large collections of processing elements can be used to achieve high-speed computations. In such designs, fault detection is required to ensure the validity of the results. The fast Hartley transform (FHT) serves for all the uses such as spectral

analysis and digital convolution to which the FFT is c ...

Keywords: Fermat number transform, Hartley transforms, VLSI, VLSI technology, algorithm-based error detection schemes, array architectures, array signal processing, built-in self test, convolution, digital convolution, digital signal processing chips, error detection, fast Hartley transform, fault detection, high-speed computations, parallel architectures, processing elements, radix-2 FHT transform, spectral analysis

16 Software reliability via run-time result-checking

Hal Wasserman, Manuel Blum
November 1997 **Journal of the ACM (JACM)**, Volume 44 Issue 6
Publisher: ACM Press

Full text available: pdf(150.60 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We review the field of result-checking, discussing simple checkers and self-correctors. We argue that such checkers could profitably be incorporated in software as an aid to efficient debugging and enhanced reliability. We consider how to modify traditional checking methodologies to make them more appropriate for use in real-time, real-number computer systems. In particular, we suggest that checkers should be allowed to use stored randomness: that is, that they should be allowed to generate ...

Keywords: Fourier transform, built-in testing, concurrent error detection, debugging, fault tolerance, result-checking, self-correcting

17 Checking approximate computations over the reals

S. Ar, M. Blum, B. Codenotti, P. Gemmell
June 1993 **Proceedings of the twenty-fifth annual ACM symposium on Theory of computing STOC '93**
Publisher: ACM Press
Full text available: pdf(847.33 KB) Additional Information: full citation, references, citings, index terms

18 Reliable System Specification for Self-Checking Data-Paths

C. Bolchini, F. Salice, D. Sciuto, L. Pomante
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 2 DATE '05**
Publisher: IEEE Computer Society
Full text available: pdf(159.26 KB) Additional Information: full citation, abstract, index terms

The design of reliable circuits has received a lot of attention in the past, leading to the definition of several design techniques introducing fault detection and fault tolerance properties in systems for critical applications/environments. Such design methodologies tackled the problem at different abstraction levels, from switch-level to logic, RT level, and more recently to system level. Aim of this paper is to introduce a novel system-level technique based on the redefinition of the operator ...

19 Self-regenerative software components

Hassen Saïdi, Bruno Dutertre, Joshua Levy, Alfonso Valdes
October 2003 **Proceedings of the 2003 ACM workshop on Survivable and self-regenerative systems: in association with 10th ACM Conference on Computer and Communications Security SSRS '03**
Publisher: ACM Press
Full text available: Additional Information:

pdf(678.94 KB) full citation, abstract, references

Self-regenerative capabilities are a new trend in survivable system design. Self-regeneration ensures the property that a system's vulnerabilities cannot be exploited to the extent that the mission objective is compromised, but instead that the vulnerabilities are eventually removed, and system functionality is restored. To establish the usefulness of self-regenerative capabilities in the design of survivable systems, it is important to ensure that a system satisfying the self-regenerative re ...

20 Finding security flaws: Combining type-based analysis and model checking for finding counterexamples against non-interference

Hiroshi Unno, Naoki Kobayashi, Akinori Yonezawa

June 2006 **Proceedings of the 2006 workshop on Programming languages and analysis for security PLAS '06**

Publisher: ACM Press

Full text available: pdf(239.70 KB) Additional Information: full citation, abstract, references, index terms

Type systems for secure information flow are useful for efficiently checking that programs have secure information flow. They are, however, conservative, so that they often reject safe programs as ill-typed. Accordingly, users have to check whether the rejected programs indeed have insecure flows. To remedy this problem, we propose a method for automatically finding a counterexample of secure information flow (input states that actually lead to leakage of secret information). Our method is a nov ...

Keywords: model checking, non-interference, type system

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